

REMARKS/ARGUMENTS

This Amendment is responsive to the Office Action mailed on March 11, 2003. A Petition for a 1-month extension of time is attached so that the due date for responding includes July 11, 2003. An RCE (request for continued examination) is also being filed concurrently herewith.

Prior to this Amendment, claims 1-43 were pending. In this Amendment, claims 1, 3, 10, 11, 22, 23, 34, 37, and 39 are amended, claims 44-45 are added, and no claims are canceled, so that claims 1-45 are pending and subject to examination on the merits.

Support for the amendments to the independent claims can be found at, for example, page 1, lines 10-15 and page 4, lines 23-27 of the specification. No new matter is added. Support for new claims 44-45 can be found at, for example, page 9, line 24 of the specification.

Claim 37 is put into independent form and pursuant to the statement at the bottom of page 15 of the Office Action, claim 37 should be allowable. Applicants sincerely and earnestly thank the Examiner for the indication of allowable subject matter.

On June 23, 2003, an interview occurred between the undersigned and the Examiner. The undersigned sincerely appreciates the Examiner's careful consideration of the arguments made during the interview.

Page 2 of the Office Action states that Figures 1 and 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated.

Applicants do not agree with this objection. However, to expedite the prosecution of the application, Applicants have labeled FIG. 1, which is discussed in the "Background of the Invention Section" as --Prior Art--, and have canceled FIG. 3. The steps shown in FIG. 3 are each recited in the application as filed and FIG. 3 is not necessary for understanding the claimed inventions. The specification has been amended to conform to the cancellation of FIG. 3.

At pages 2-3 of the Office Action, claims 3, 10, 11, and 34 are objected to as they allegedly lack antecedent basis. At pages 4-5 of the Office Action, claims 3, 10, 11, and 34 are correspondingly rejected under 35 USC 112, 2nd paragraph for allegedly being indefinite.

Applicants do not agree with the claim objections and claim rejections. However, to expedite the prosecution of the application, Applicants have amended claims 3, 10, 11, and 34. Accordingly, withdrawal of the claim objections and claim rejections is requested.

At the bottom of page 3 of the Office Action, claim 11 is objected to as being a duplicate of claim 10.

In response, claim 11 is amended to depend from dependent claim 4 so it is no longer the same as claim 10. Withdrawal of the objection is requested.

35 USC 103

Annapragada et al. (U.S. Patent No. 6,410,221) and Forbes et al. (U.S. Patent No. 5,926,740)

Claims 1, 10, 11, 17-19, 23, 26, 29, and 28 are rejected as being obvious in view of Annapragada et al. and Forbes et al. According to the Examiner:

Annapragada discloses forming an extremely low dielectric constant (ELK) film (22) on a substrate (20). ... Annapragada does not disclose forming an amorphous silicon carbide capping layer on [an] ELK film. Forbes discloses a photolithography process wherein an antireflective coating is deposited between the layer to be etched and the photoresist mask layer. The antireflective coating (ARC) comprises a bottom layer of amorphous silicon carbide (105) and an upper layer of silicon oxycarbide (110) (col. 8, ln. 46-col. 9, ln 60). Forbes discloses that this antireflective coating is extremely useful in preventing light from the photolithography process from reaching the underlying material, whereby the resolution of the photolithography process is greatly improved, resulting in higher density circuits being able to be formed (col. 3, ln. 26-50). Forbes states that this ARC layer is appropriate to use in the formation of interconnection layers wherein underlying metal is usually highly reflective (col. 3, ln. 40-47). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the ARC film of Forbes when conducting the photolithography process of etching the ELK layer of Annapragada because Forbes teaches that the ARC layer advantageously improves the quality of a photolithography

process, thereby allowing higher density devices to be formed. Furthermore, Annapragada states that the material underlying the photoresist includes metal (124) and Forbes discloses that the ARC is especially useful when underlying materials include metal, which is highly reflective.

Obviousness has not been established, since each and every limitation is not taught or suggested by the cited art. To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Here, neither Annapragada et al. nor Forbes et al. teach or suggest a process or a stack including an amorphous silicon carbide capping layer and/or a carbon doped oxide layer that is on an ELK film that “remains in” a semiconductor device as recited in independent claims 1, 22, 23, and 39.

As noted in the Office Action, Annapragada et al. fails to mention or suggest any silicon carbide capping layer. Forbes et al. is relied upon to supplement the deficiencies of Annapragada et al. In particular, the Examiner relies on the antireflective coating 105 and an upper layer of silicon oxycarbide 110 as respectively being the “amorphous silicon carbide capping layer” and the “carbon-doped oxide layer” in the claims (see, *e.g.*, dependent claim 2). The Examiner acknowledges that layers 105 and 110 in Forbes et al. are “anti-reflective coatings” or ARCs.

Forbes et al. does not teach or suggest that the ARC layers 105 and 110 should remain in a semiconductor device. A general textbook on semiconductor processing at the time of the present invention indicates that ARCs are typically removed after they are used and are not in a semiconductor device. According to pages 292-293 of *Microchip Fabrication* by Peter Van Zant (1997), a textbook on semiconductor processing (attached hereto), an ARC is used in masking processes, and provides advantages including planarizing a resist layer and cutting down on light scattering. An ARC is spun onto a wafer and is baked. After a resist is spun on top of the ARC, the wafer is aligned and exposed in a pattern. The pattern is developed in both the resist and the ARC. The textbook states “the ARC must develop and be stripped with the same chemicals as the resist” (see page 293). The textbook suggests that at the time of the

invention, one skilled in the art would have typically stripped ARCs like those described in Forbes, et al. and would not have left them in a formed semiconductor device. Accordingly, since Forbes et al. fails to teach or suggest that his silicon carbide and silicon oxycarbide ARC layers are left in a semiconductor device, the obviousness rejection should be withdrawn for this reason alone.

Annapragada et al., Forbes et al., and Xu et al.

Claims 3-9, 22, 30, 35, and 36 are rejected as obvious in view of Annapragada et al., Forbes et al., and Xu et al.

The combination of Annapragada et al. and Forbes et al. is improper for the reasons provided above. The additional citation of Xu et al. fails to remedy the deficiencies of Annapragada et al. and Forbes et al.

In addition, in this obviousness rejection, the Examiner states that “it would have been obvious to one of ordinary skill in the art to use the methods disclosed by Xu et al. to deposit the silicon carbide layer of Forbes et al., because Xu et al. “teach that by depositing a silicon carbide layer according to their process, the layer advantageously has a lower dielectric constant, lower leakage current, higher breakdown strength, and is easier to etch than conventional SiC that is deposited using silane and methane.”

The combination of Annapragada et al., Forbes et al., and Xu et al. was based on improper hindsight. Care must be taken to avoid hindsight reconstruction by using the patent application as a guide through the maze of prior art references, combining the right references in the right way so as to achieve the result of the claims. *Grain Processing Corp. v. American Maize-Products Co.*, 840 F.2d 902, 907, 5 USPQ2d 1788, 1792 (Fed. Cir. 1988). The Examiner alleges that the silicon carbide and silicon oxycarbide ARCs of Forbes et al. “improve the quality of a photolithography process”, while also alleging that one would have substituted Xu et al.’s silicon carbide layer for the ARCs in Forbes et al. to provide a lower dielectric constant, lower leakage current, higher breakdown strength, and easier etching. Clearly, one skilled in the art would not have been motivated to replace the silicon carbide layers in Forbes et al. with the

silicon carbide layer in Xu et al. for the reason provided by the Examiner, since none of the properties mentioned in Xu et al. are particularly pertinent to the function or the properties of the ARCs described in Forbes et al. Accordingly, the additional citation of Xu et al. in combination with Annapragada et al. and Forbes et al. is especially improper.

Annapragada et al., Forbes et al., Xu et al., and Lobada et al.

Claims 12-16, 24, and 25 are rejected as obvious in view of Annapragada et al., Forbes et al., Xu et al., and Lobada et al.

This rejection is traversed. As explained above, the combination of Annapragada et al., Forbes et al., and Xu et al. is improper. The additional citation of Lobada et al. fails to remedy the deficiencies of Annapragada et al., Forbes et al., and Xu et al. Withdrawal of the obviousness rejection is requested.

Annapragada et al., Forbes et al., and Lobada et al.

Claims 20, 21, and 31 are rejected as obvious in view of Annapragada et al., Forbes et al., and Lobada et al. This rejection is traversed.

The combination of Annapragada et al. and Forbes et al. is improper for the reasons provided above. The additional citation of Lobada et al. fails to remedy the deficiencies of Annapragada et al. and Forbes et al.

Annapragada et al., Forbes et al., Xu et al., and Lobada et al.

Claims 2, 32, 33, and 39-43 are rejected as obvious in view of Annapragada et al., Forbes et al., and Lobada et al. This rejection is traversed.

The combination of Annapragada et al., Forbes et al., and Xu et al. is improper for the reasons provided above. The additional citation of Lobada et al. fails to remedy the deficient combination of Annapragada et al., Forbes et al., and Xu et al.

Appl. No. 09/692,527
Amdt. dated July 11, 2003
Reply to Office Action of March 11, 2003

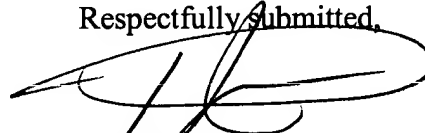
PATENT

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

A handwritten signature in black ink, appearing to be "Patrick R. Jewik", written over a horizontal line.

Patrick R. Jewik
Reg. No. 40,456

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: 415-576-0200
Fax: 415-576-0300
PRJ:prj
SF 1472719 v1

Other Reference Books of Interest by McGraw-Hill

Handbooks

BERNSEN • *Television Engineering Handbook*
CHEN • *Computer Engineering Handbook*
COOMBS • *Printed Circuits Handbook*
DI GIACOMO • *Digital Bus Handbook*
DI GIACOMO • *VLSI Handbook*
PINE AND CHRISTIANSEN • *Electronics Engineers' Handbook*
HARPER • *Electronic Packaging and Interconnection Handbook*
JUBAN AND GERVA • *Juran's Quality Control Handbook*
BORBAUGH • *Digital Filter Designer's Handbook*
SERRENT AND HARPER • *Hybrid Microelectronic Handbook*
TAYLOR • *Engineering Mathematics Handbook*
WILSON • *Electro-Optics Handbook*
WILSON AND TAYLOR • *Electronic Filter Design Handbook*

Other

ANTONINETTI • *Power Integrated Circuits*
ANTONINETTI AND MASSOBRO • *Semiconductor Device Modeling with SPICE*
BEST • *Phase-Locked Loops*
BUCHANAN • *CMOS/TTL Digital Systems Design*
BUCHANAN • *BiCMOS/CMOS Systems Design*
BYRDS • *Printed Circuit Board Design with Microcomputers*
ELLIOTT • *Integrated Circuits Fabrication Technology*
HECHT • *The Laser Guidebook*
KORLOVSKI • *Inside SPICE*
SMITH • *Thin-Film Deposition*
SZE • *VLSI Technology*
SZE • *Mixed Analog Digital VLSI Devices and Technology: An Introduction*
• *LSI/VLSI Testability Design*
WOBESCHALL • *Circuit Design for Electronic Instrumentation*
WYATT • *Electro-Optical System Design*

To order or receive additional information on these or any other McGraw-Hill titles, please call 1-800-822-8168 in the United States. In other countries, contact your local McGraw-Hill representative.

KEY = WM16XXA

Microchip Fabrication

A Practical Guide to Semiconductor Processing

Peter Van Zant

Third Edition

McGraw-Hill

New York San Francisco Washington, D.C. Auckland Bogota
Caracas Lisbon London Madrid Mexico City Milan
Montreal New Delhi San Juan Singapore
Sydney Tokyo Toronto

Library of Congress Cataloging-in-Publication Data

Van Zant, Peter.

Microchip fabrication : a practical guide to semiconductor processing / Peter Van Zant.—3rd ed.

p. cm.

Includes index.

ISBN 0-07-067250-4 (hardcover)

1. Semiconductors—Design and construction. I. Title.

DN PROCESS

621.38152—dc20

96-15729
CIP

McGraw-Hill

A Division of The McGraw-Hill Companies



Copyright © 1997 by The McGraw-Hill Companies, Inc. All rights reserved. Printed in the United States of America. Except as permitted under the United States Copyright Act of 1976, no part of this publication may be reproduced or distributed in any form or by any means, or stored in a data base or retrieval system, without the prior written permission of the publisher.

5 6 7 8 9 0 DOC/DOC 9 0 1 0 9 8

ISBN 0-07-067250-4

The sponsoring editor for this book was Steve Chapman, the editing supervisor was Fred Bernardi, and the production supervisor was Pamela Pelton. It was set in Century Schoolbook by Dina E. John of McGraw-Hill's Professional Book Group composition unit.

Printed and bound by R. R. Donnelley & Sons Company.

 This book is printed on recycled, acid-free paper containing a minimum of 50% recycled, de-inked fiber.

Information contained in this work has been obtained by The McGraw-Hill Companies, Inc. ("McGraw-Hill") from sources believed to be reliable. However, neither McGraw-Hill nor its authors guarantees the accuracy or completeness of any information published herein and neither McGraw-Hill nor its authors shall be responsible for any errors, omissions, or damages arising out of use of this information. This work is published with the understanding that McGraw-Hill and its authors are supplying information but are not attempting to render engineering or other professional services. If such services are required, the assistance of an appropriate professional should be sought.

INTERNATIONAL EDITION

Copyright ©1997. Exclusive rights by The McGraw-Hill Companies, Inc. for manufacture and export. This book cannot be re-exported from the country to which it is assigned by McGraw-Hill. The International Edition is not available in North America.

When ordering this title, use ISBN 0-07-114837-X.

To the wonderfully creative, dedicated, and hard-playing band of chip pioneers who created the world's most advanced manufacturing process, transforming Silicon Valley into the Florence of the twentieth century. And to the spirit of Marchetti's and the Wagon Wheel.

The amount of diffusion is in proportion to the resist thickness. Some additives put in the photoresist to increase radiation absorption also increase the amount of radiation diffusion, thus reducing image resolution.

Subsurface reflectivity

The high-intensity exposing radiation ideally is directed at a 90° angle to the wafer surface. When this ideal situation exists, exposing waves reflect directly up and down in the resist, leaving a well-defined exposed image (Fig. 10.7). In reality, some of the exposing waves are traveling at angles other than 90° and expose unwanted portions of the resist.

This subsurface reflectivity varies with the surface layer material and the surface smoothness. Metal layers, especially aluminum and aluminum alloys, have higher reflectivity properties. A goal of the deposition processes is a consistent and smooth surface to control this form of reflection.

Reflection problems are intensified on wafers with many steps, also called a varied topography. The sidewalls of the steps reflect radiation at angles into the resist, causing poor image resolution. A particular problem is light interference at the step that causes a "notching" of the pattern as it crosses the step (Fig. 10.8).

Antireflective Coatings

Antireflective coatings (ARCs) spun onto the wafer surface before the resist (Fig. 10.9) can aid the patterning of small images. The ARC layer brings several advantages to the masking process. First is a planarizing of the surface, which makes for a more planarized resist layer. Second, an ARC cuts down on light scattering from the surface into the resist, which helps in the definition of small images. An ARC can also minimize standing wave effects and improve the image contrast. The latter benefit comes from increased exposure latitude with a proper ARC.

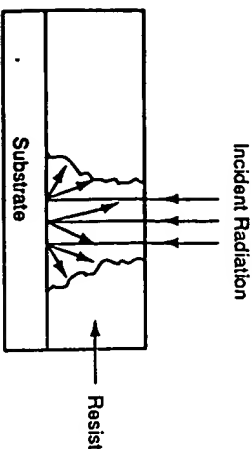


Figure 10.7 Subsurface reflectivity.

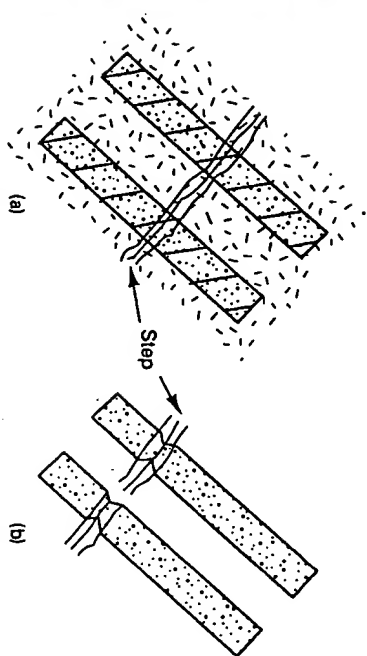


Figure 10.8 Metal line "notching" over step. (a) Before etch; (b) after etch.

An ARC is spun onto the wafer and baked. After the resist is spun on top of the ARC, the wafer is aligned and exposed. The pattern is developed in both the resist and the ARC. During the etch, the ARC acts as an etch barrier. To be effective, an ARC material must transmit light in the same range as the resist. It must also have good adhesion properties with the wafer surface and the resist. Two other requirements are that the ARC must have a refractive index that matches the resist, and that the ARC must develop and be stripped with the same chemicals as the resist.

There are several penalties associated with the use of an ARC. One is an additional layer requiring a separate spin and bake. The resolution gains offered by an ARC can be offset with poor thickness control and/or with an ill-controlled developing step. The time of exposure can increase 30 to 50 percent, increasing the wafer throughput time. ARC layers may also be used as the intermediate layer in a tri-layer resist process or used on the top of the photoresist, called a top antireflective coating or TAR.

Standing waves

In "Subsurface reflectivity," it was mentioned that the ideal exposure situation is when the radiation waves are directed to the wafer surface at 90°. This is true when only reflection problems are under consideration. However, 90° reflection causes another problem in positive photoresists, the creation of standing waves. As the radiation wave reflects off the surface and travels back up through the resist, it interferes constructively and destructively with the incoming wave, creating regions of varying energy (Fig. 10.10). The result after development is a rippled sidewall and a loss of resolution. A number of solutions are used to moderate standing waves, including dyes in the resist and separate